

# NLAS324

## Dual SPST Analog Switch, Low Voltage, Single Supply

The NLAS324 is a dual SPST (Single Pole, Single Throw) switch, similar to 1/2 a standard 4066. The device permits the independent selection of 2 analog/digital signals. Available in the Ultra-Small 8 package.

The use of advanced 0.6  $\mu$  CMOS process, improves the  $R_{ON}$  resistance considerably compared to older higher voltage technologies.

### Features

- On Resistance is 20  $\Omega$  Typical at 5.0 V
- Matching is  $< 1 \Omega$  Between Sections
- 2 – 6 V Operating Range
- Ultra Low  $< 5$  pC Charge Injection
- Ultra Low Leakage  $< 1$  nA at 5.0 V, 25°C
- Wide Bandwidth  $> 200$  MHz,  $-3$  dB
- 2000 V ESD (HBM)
- Ron Flatness  $\pm 6 \Omega$  at 5.0 V
- US8 Package
- Negative Enable
- Switches are Independent
- Pb-Free Package is Available

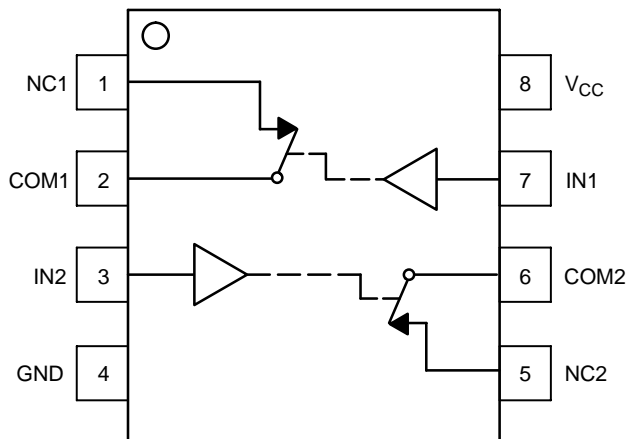


Figure 1. Pinout



**ON Semiconductor®**

<http://onsemi.com>

### MARKING DIAGRAM



A7 = Device Code  
M = Date Code\*  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

\*Date Code orientation may vary depending upon manufacturing location.

### PIN ASSIGNMENT

1	NC1
2	COM1
3	IN2
4	GND
5	NC2
6	COM2
7	IN1
8	V <sub>CC</sub>

### FUNCTION TABLE

On/Off Enable Input	State of Analog Switch
L	On
H	Off

### ORDERING INFORMATION

Device	Package	Shipping†
NLAS324US	US8	3,000 / Tape & Reel
NLAS324USG	US8 (Pb-Free)	3,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

**MAXIMUM RATINGS**

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage	-0.5 to +7.0	V
V <sub>I</sub>	DC Input Voltage	-0.5 to +7.0	V
V <sub>O</sub>	DC Output Voltage	-0.5 to +7.0	V
I <sub>IK</sub>	DC Input Diode Current V <sub>I</sub> < GND	-50	mA
I <sub>OK</sub>	DC Output Diode Current V <sub>O</sub> < GND	-50	mA
I <sub>O</sub>	DC Output Sink Current	±50	mA
I <sub>CC</sub>	DC Supply Current per Supply Pin	±100	mA
I <sub>GND</sub>	DC Ground Current per Ground Pin	±100	mA
T <sub>STG</sub>	Storage Temperature Range	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C
T <sub>J</sub>	Junction Temperature under Bias	+150	°C
θ <sub>JA</sub>	Thermal Resistance (Note 1)	250	°C/W
P <sub>D</sub>	Power Dissipation in Still Air at 85°C	250	mW
MSL	Moisture Sensitivity	Level 1	
F <sub>R</sub>	Flammability Rating Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in	
V <sub>ESD</sub>	ESD Withstand Voltage Human Body Model (Note 2) Machine Model (Note 3) Charged Device Model (Note 4)	> 2000 > 150 N/A	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Measured with minimum pad spacing on an FR4 board, using 10 mm-by-1 inch, 2-ounce copper trace with no air flow.
2. Tested to EIA/JESD22-A114-A.
3. Tested to EIA/JESD22-A115-A.
4. Tested to JESD22-C101-A.

**RECOMMENDED OPERATING CONDITIONS**

Symbol	Characteristics	Min	Max	Unit
V <sub>CC</sub>	Positive DC Supply Voltage	2.0	5.5	V
V <sub>IN</sub>	Digital Input Voltage (Enable)	GND	5.5	V
V <sub>IO</sub>	Static or Dynamic Voltage Across an Off Switch	GND	V <sub>CC</sub>	V
V <sub>IS</sub>	Analog Input Voltage (NO, COM)	GND	V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature Range, All Package Types	-55	+125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise or Fall Time, (Enable Input) V <sub>CC</sub> = 3.3 V ± 0.3 V V <sub>CC</sub> = 5.0 V ± 0.5 V	0	100	ns/V
		0	20	

**DEVICE JUNCTION TEMPERATURE VERSUS TIME TO 0.1% BOND FAILURES**

Junction Temperature °C	Time, Hours	Time, Years
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.4
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

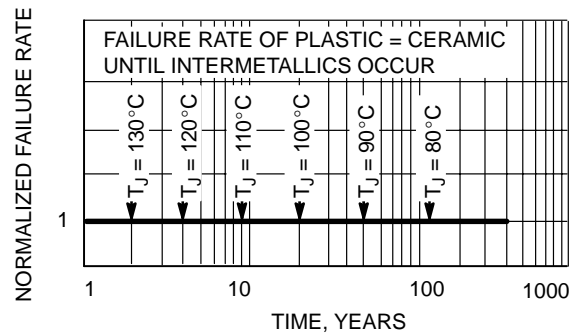


Figure 2. Failure Rate vs. Time Junction Temperature

# NLAS324

## DC CHARACTERISTICS – Digital Section (Voltages Referenced to GND)

Symbol	Parameter	Condition	V <sub>CC</sub>	Guaranteed Max Limit			Unit
				-55 to 25°C	<85°C	<125°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage, Enable Inputs		2.0	1.5	1.5	1.5	V
			3.0	2.1	2.1	2.1	
			4.5	3.15	3.15	3.15	
			5.5	3.85	3.85	3.85	
V <sub>IL</sub>	Maximum Low-Level Input Voltage, Enable Inputs		2.0	0.5	0.5	0.5	V
			3.0	0.9	0.9	0.9	
			4.5	1.35	1.35	1.35	
			5.5	1.65	1.65	1.65	
I <sub>IN</sub>	Maximum Input Leakage Current, Enable Inputs	V <sub>IN</sub> = 5.5 V or GND	0 V to 5.5 V	±0.1	±1.0	±1.0	µA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per package)	Enable and V <sub>IS</sub> = V <sub>CC</sub> or GND	5.5	1.0	1.0	2.0	µA

## DC ELECTRICAL CHARACTERISTICS – Analog Section

Symbol	Parameter	Condition	V <sub>CC</sub>	Guaranteed Max Limit			Unit
				-55 to 25°C	<85°C	<125°C	
R <sub>ON</sub>	Maximum ON Resistance (Figures 8 – 12)	V <sub>IN</sub> = V <sub>IH</sub> V <sub>IS</sub> = V <sub>CC</sub> to GND  I <sub>IS</sub>   ≤ 10.0mA	3.0	45	50	55	Ω
			4.5	30	35	40	
			5.5	25	30	35	
R <sub>FLAT(ON)</sub>	ON Resistance Flatness	V <sub>IN</sub> = V <sub>IH</sub>  I <sub>IS</sub>   ≤ 10.0mA V <sub>IS</sub> = 1V, 2V, 3.5V	4.5	4	4	5	Ω
I <sub>NO(OFF)</sub>	Off Leakage Current, Pin 2 (Figure 3)	V <sub>IN</sub> = V <sub>IL</sub> V <sub>NO</sub> = 1.0 V, V <sub>COM</sub> = 4.5 V or V <sub>COM</sub> = 1.0 V and V <sub>NO</sub> 4.5 V	5.5	1	10	100	nA
I <sub>COM(OFF)</sub>	Off Leakage Current, Pin 1 (Figure 3)	V <sub>IN</sub> = V <sub>IL</sub> V <sub>NO</sub> = 4.5 V or 1.0 V V <sub>COM</sub> = 1.0 V or 4.5 V	5.5	1	10	100	nA

## AC ELECTRICAL CHARACTERISTICS (Input t<sub>r</sub> = t<sub>f</sub> = 3.0 ns)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> (V)	Guaranteed Max Limit									Unit
				-55 to 25°C			<85°C			<125°C			
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t <sub>ON</sub>	Turn-On Time	R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 35 pF (Figures 4, 5, and 13)	2.03.04.55.5		7.0	14			16			16	ns
					5.0	10			12			12	
					4.5	9			11			11	
					4.5	9			11			11	
t <sub>OFF</sub>	Turn-Off Time	R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 35 pF (Figures 4, 5, and 13)	2.03.04.5 5.5		11.0	22			24			24	ns
					7.0	14			16			16	
					5.0	10			12			12	
					5.0	10			12			12	

			Typical @ 25, V <sub>CC</sub> = 5.0 V									
C <sub>IN</sub>	Maximum Input Capacitance, Select Input		8									pF
C <sub>NO</sub> or C <sub>N</sub> C	Analog I/O (switch off)		10									
C <sub>COM(OFF)</sub>	Common I/O (switch off)		10									
C <sub>COM(ON)</sub>	Feedthrough (switch on)		20									

# NLAS324

## ADDITIONAL APPLICATION CHARACTERISTICS (Voltages Referenced to GND Unless Noted)

Symbol	Parameter	Condition	V <sub>CC</sub> V	Limit	Unit
				25°C	
BW	Maximum On-Channel -3dB Bandwidth or Minimum Frequency Response	V <sub>IS</sub> = 0 dBm V <sub>IS</sub> centered between V <sub>CC</sub> and GND (Figures 6 and 14)	3.0 4.5 5.5	190 200 220	MHz
V <sub>ONL</sub>	Maximum Feedthrough On Loss	V <sub>IS</sub> = 0 dBm @ 10 kHz V <sub>IS</sub> centered between V <sub>CC</sub> and GND (Figure 6)	3.0 4.5 5.5	-2 -2 -2	dB
V <sub>ISO</sub>	Off-Channel Isolation	f = 100 kHz; V <sub>IS</sub> = 1 V RMS V <sub>IS</sub> centered between V <sub>CC</sub> and GND (Figures 6 and 15)	3.0 4.5 5.5	-93	dB
Q	Charge Injection Enable Input to Common I/O	V <sub>IS</sub> = V <sub>CC</sub> to GND, F <sub>IS</sub> = 20 kHz t <sub>r</sub> = t <sub>f</sub> = 3 ns R <sub>IS</sub> = 0 Ω, C <sub>L</sub> = 1000 pF Q = C <sub>L</sub> * ΔV <sub>OUT</sub> (Figures 7 and 16)	3.0 5.5	1.5 3.0	pC
THD	Total Harmonic Distortion THD + Noise	F <sub>IS</sub> = 20 Hz to 1 MHz, R <sub>L</sub> = R <sub>gen</sub> = 600 Ω, C <sub>L</sub> = 50 pF V <sub>IS</sub> = 3.0 V <sub>PP</sub> sine wave V <sub>IS</sub> = 5.0 V <sub>PP</sub> sine wave (Figure 17)	3.3 5.5	0.3 0.15	%

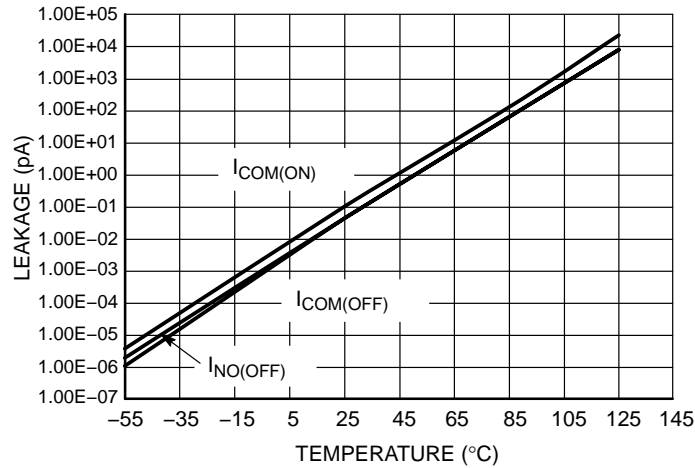


Figure 3. Switch Leakage vs. Temperature

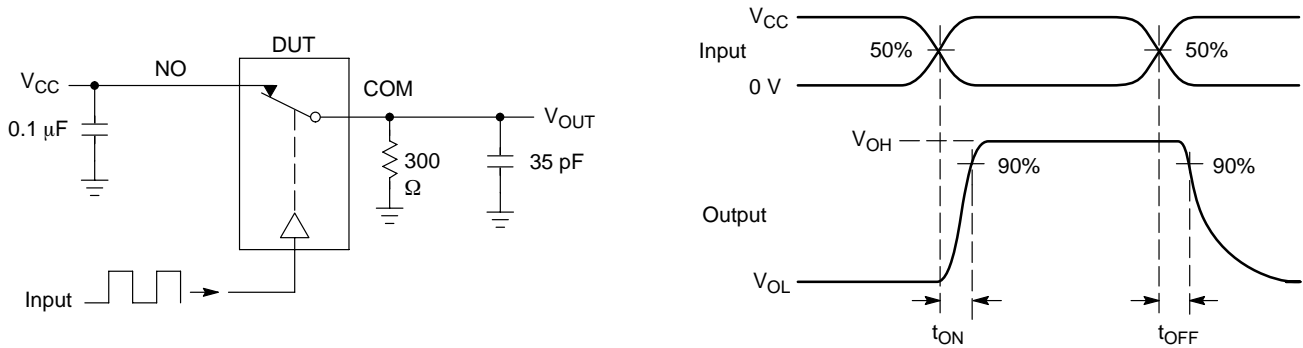


Figure 4. t<sub>ON</sub>/t<sub>OFF</sub>

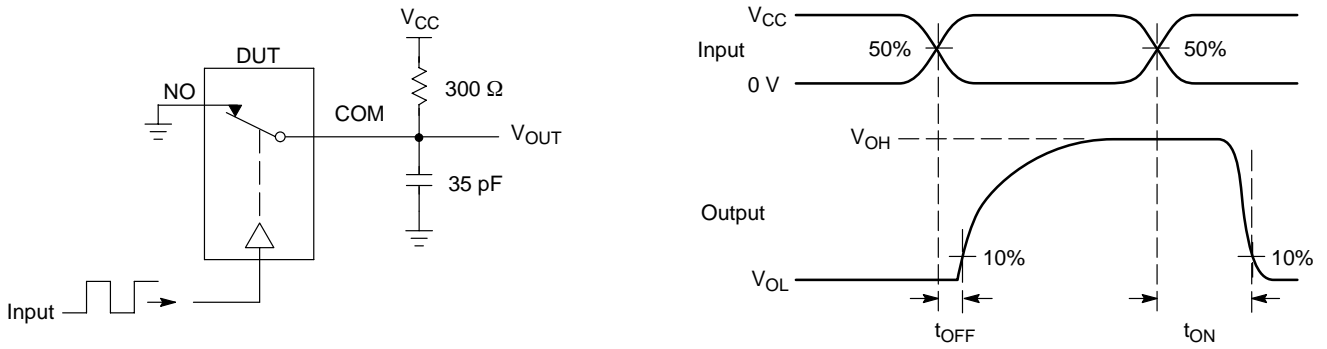
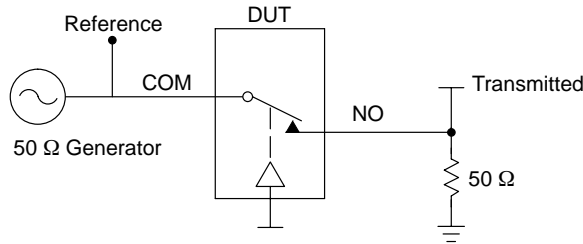


Figure 5.  $t_{ON}/t_{OFF}$



Channel switch control/s test socket is normalized. Off isolation is measured across an off channel. On loss is the bandwidth of an On switch.  $V_{ISO}$ , Bandwidth and  $V_{ONL}$  are independent of the input signal direction.

$$V_{ISO} = \text{Off Channel Isolation} = 20 \text{ Log} \left( \frac{V_{OUT}}{V_{IN}} \right) V_{IN} \text{ at } 100 \text{ kHz}$$

$$V_{ONL} = \text{On Channel Loss} = 20 \text{ Log} \left( \frac{V_{OUT}}{V_{IN}} \right) V_{IN} \text{ at } 100 \text{ kHz to } 50 \text{ MHz}$$

Bandwidth (BW) = the frequency 3 dB below  $V_{ONL}$

Figure 6. Off Channel Isolation/On Channel Loss (BW)/Crosstalk (On Channel to Off Channel)/ $V_{ONL}$

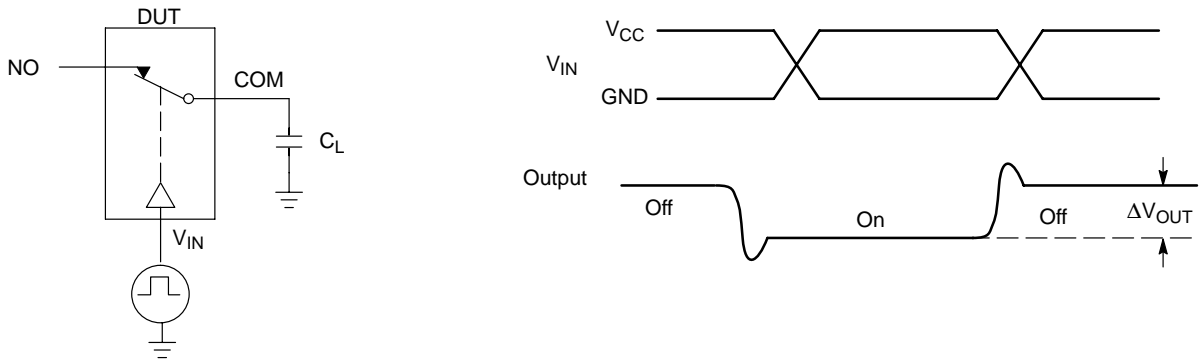


Figure 7. Charge Injection: (Q)

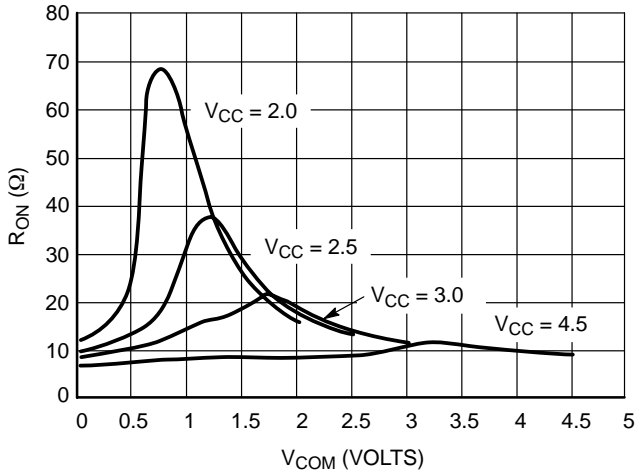


Figure 8.  $R_{ON}$  vs.  $V_{COM}$  and  $V_{CC}$  (@25°C)

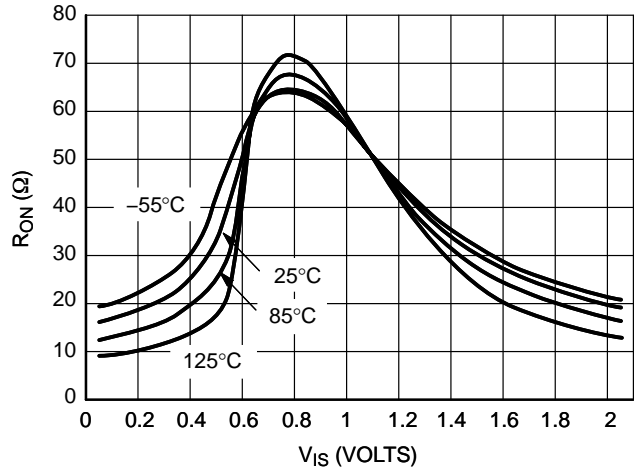


Figure 9.  $R_{ON}$  vs.  $V_{COM}$  and Temperature,  $V_{CC} = 2.0$  V

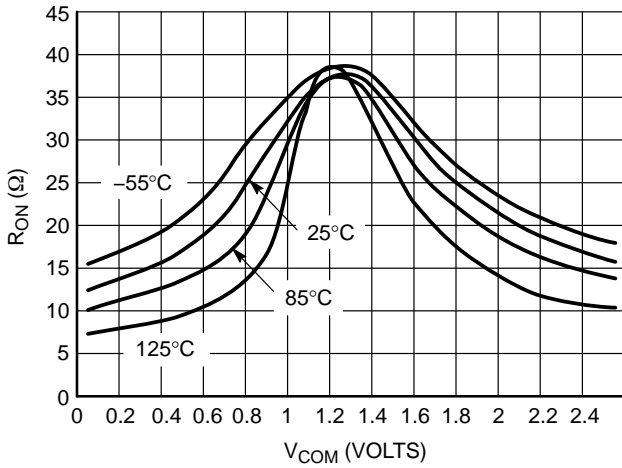


Figure 10.  $R_{ON}$  vs.  $V_{COM}$  and Temperature,  $V_{CC} = 2.5$  V

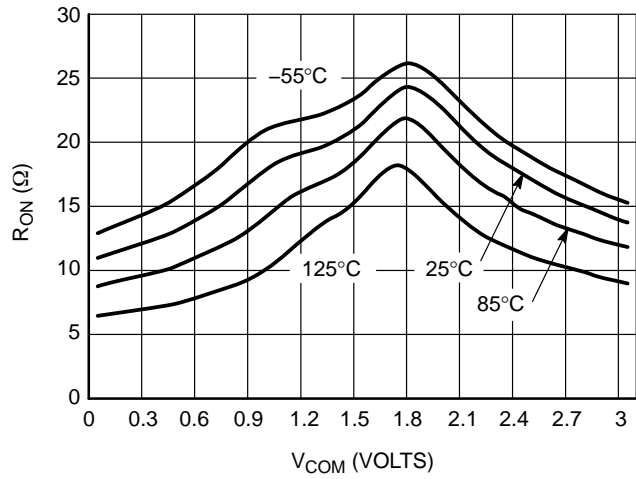


Figure 11.  $R_{ON}$  vs.  $V_{COM}$  and Temperature,  $V_{CC} = 3.0$  V

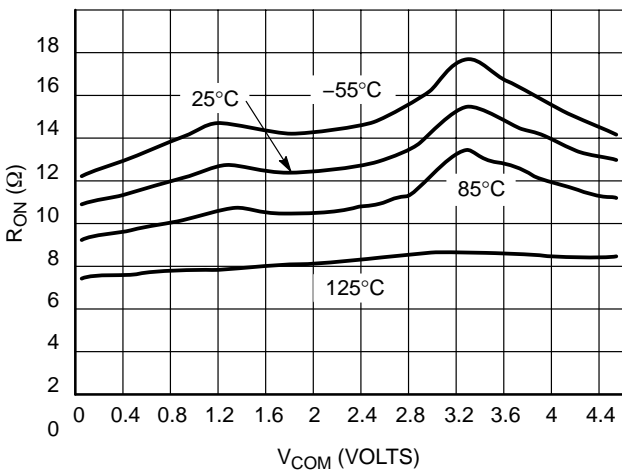


Figure 12.  $R_{ON}$  vs.  $V_{COM}$  and Temperature,  $V_{CC} = 4.5$  V

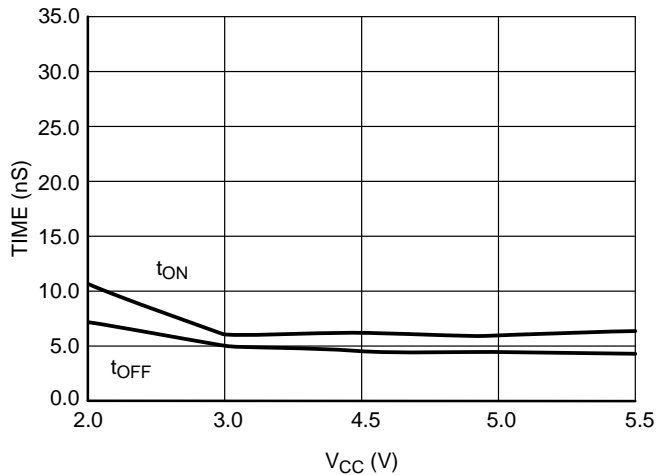


Figure 13. Switching Time vs. Supply Voltage,  $T = 25^\circ\text{C}$

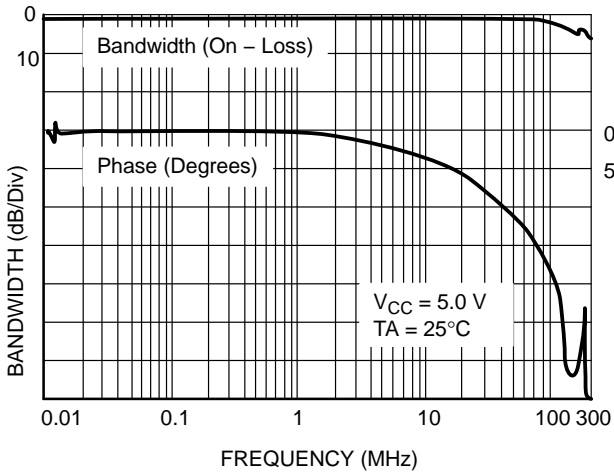


Figure 14. ON Channel Bandwidth and Phase Shift Over Frequency

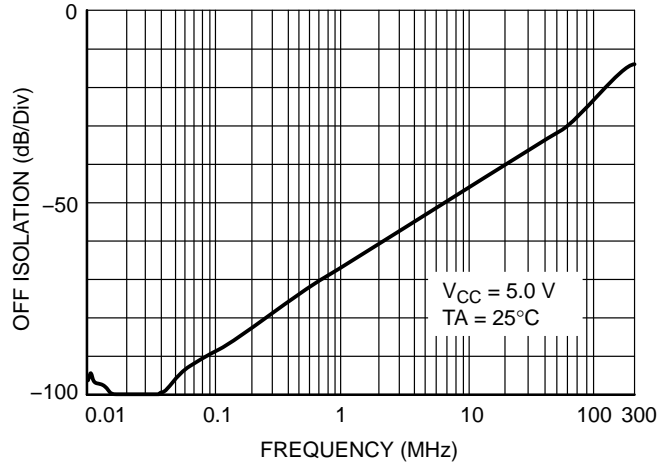


Figure 15. Off Channel Isolation

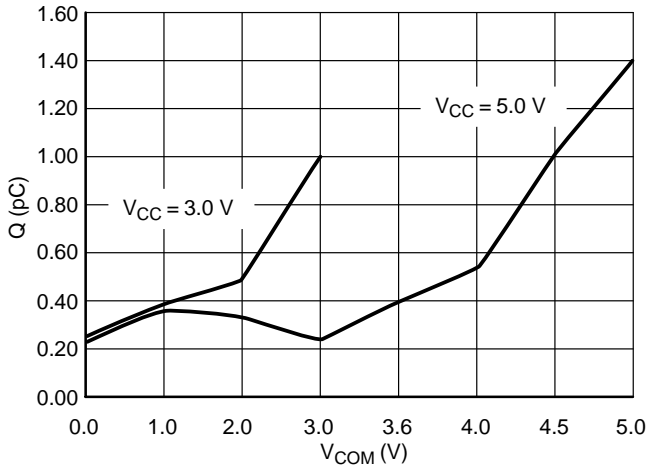


Figure 16. Charge Injection vs.  $V_{COM}$

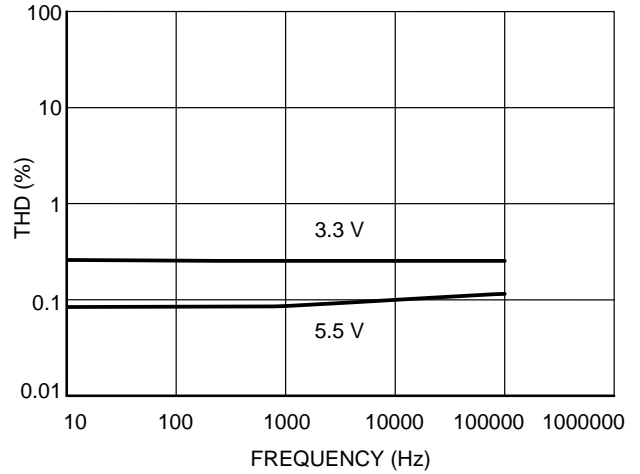


Figure 17. THD vs. Frequency

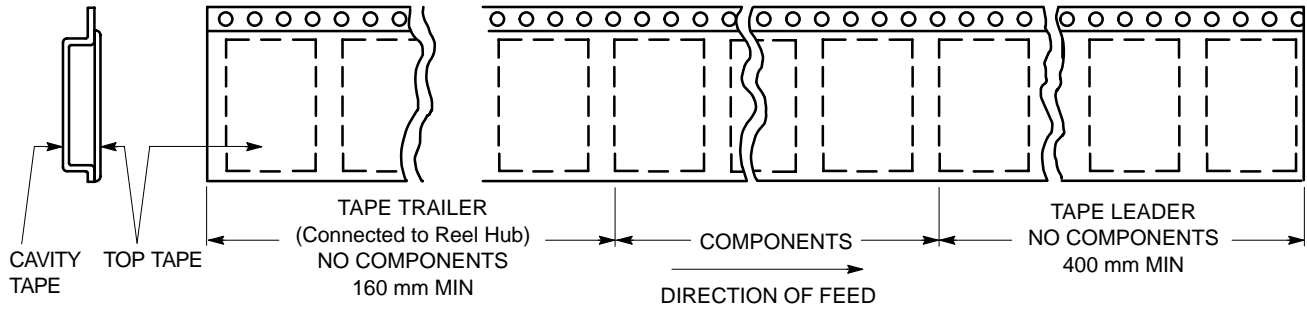


Figure 18. Tape Ends for Finished Goods

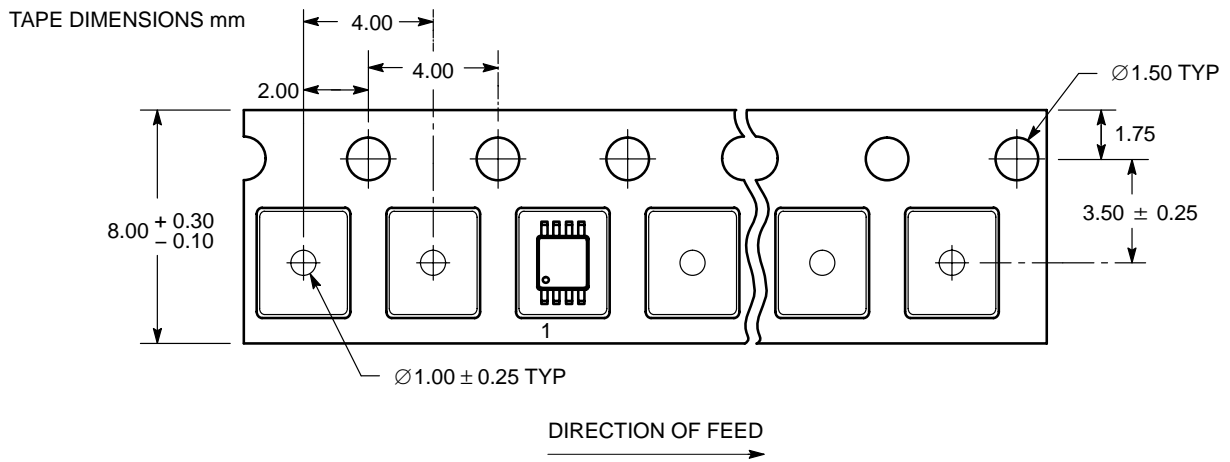


Figure 19. US8 Reel Configuration/Orientation



# NLAS324

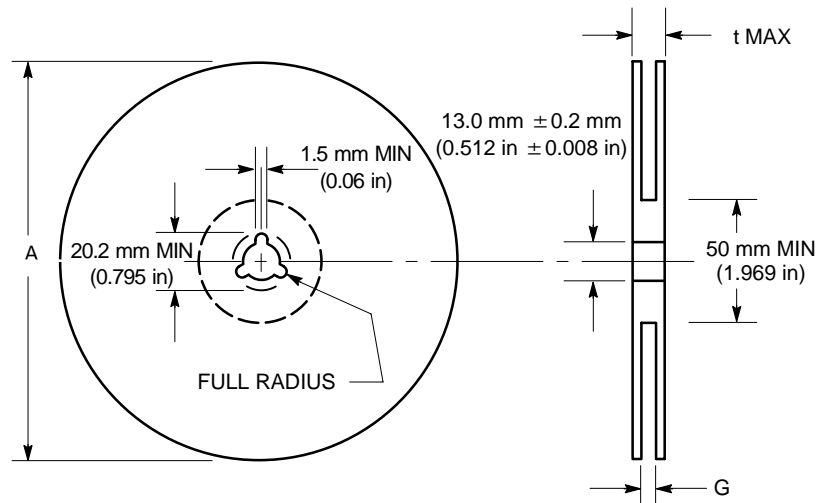


Figure 20. Reel Dimensions

## REEL DIMENSIONS

Tape Size	T and R Suffix	A Max	G	t Max
8 mm	US	178 mm (7 in)	8.4 mm, + 1.5 mm, -0.0 (0.33 in + 0.059 in, -0.00)	14.4 mm (0.56 in)

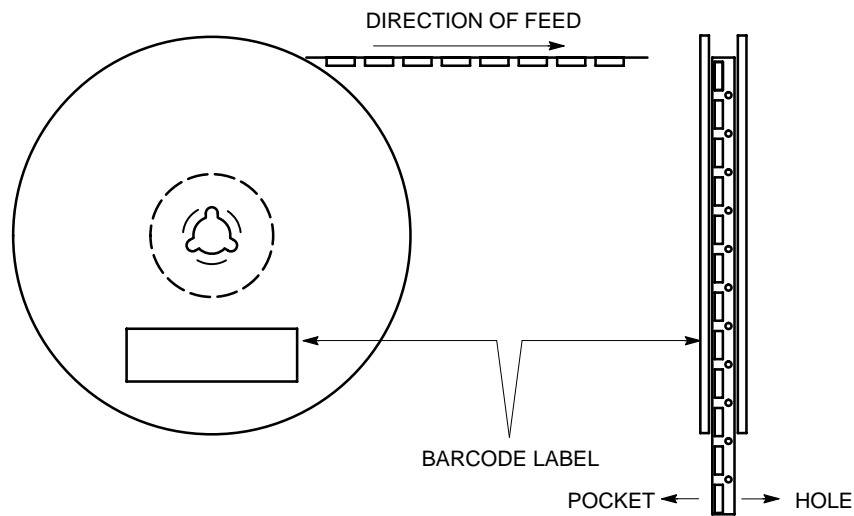
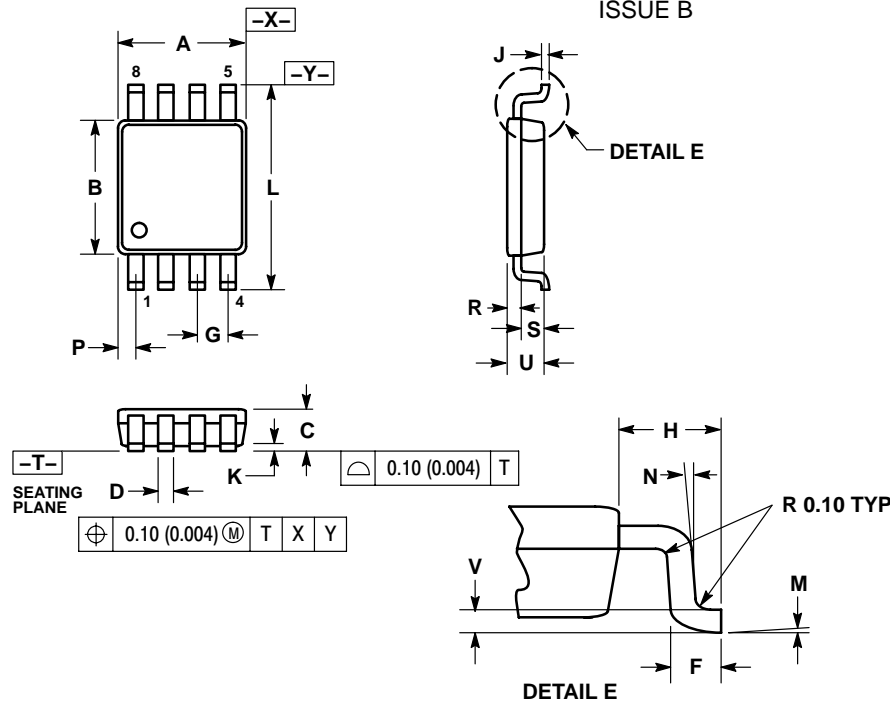


Figure 21. Reel Winding Direction

# NLAS324

## PACKAGE DIMENSIONS

US8  
US SUFFIX  
CASE 493-02  
ISSUE B

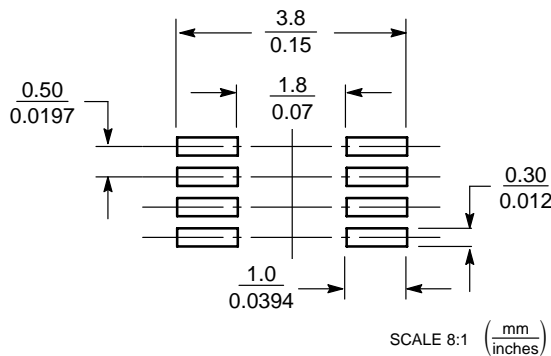


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION "A" DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR. MOLD FLASH, PROTRUSION AND GATE BURR SHALL NOT EXCEED 0.140 MM (0.0055") PER SIDE.
4. DIMENSION "B" DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSION. INTER-LEAD FLASH AND PROTRUSION SHALL NOT EXCEED 0.140 (0.0055") PER SIDE.
5. LEAD FINISH IS SOLDER PLATING WITH THICKNESS OF 0.0076-0.0203 MM. (300-800 °).
6. ALL TOLERANCE UNLESS OTHERWISE SPECIFIED ±0.0508 (0.0002 °).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.90	2.10	0.075	0.083
B	2.20	2.40	0.087	0.094
C	0.60	0.90	0.024	0.035
D	0.17	0.25	0.007	0.010
F	0.20	0.35	0.008	0.014
G	0.50 BSC		0.020 BSC	
H	0.40 REF		0.016 REF	
J	0.10	0.18	0.004	0.007
K	0.00	0.10	0.000	0.004
L	3.00	3.20	0.118	0.126
M	0 °	6 °	0 °	6 °
N	5 °	10 °	5 °	10 °
P	0.23	0.34	0.010	0.013
R	0.23	0.33	0.009	0.013
S	0.37	0.47	0.015	0.019
U	0.60	0.80	0.024	0.031
V	0.12 BSC		0.005 BSC	

### SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

### PUBLICATION ORDERING INFORMATION

**LITERATURE FULFILLMENT:**  
Literature Distribution Center for ON Semiconductor  
P.O. Box 61312, Phoenix, Arizona 85062-1312 USA  
**Phone:** 480-829-7710 or 800-344-3860 Toll Free USA/Canada  
**Fax:** 480-829-7709 or 800-344-3867 Toll Free USA/Canada  
**Email:** orderlit@onsemi.com

**N. American Technical Support:** 800-282-9855 Toll Free USA/Canada

**Japan:** ON Semiconductor, Japan Customer Focus Center  
2-9-1 Kamimeguro, Meguro-ku, Tokyo, Japan 153-0051  
**Phone:** 81-3-5773-3850

**ON Semiconductor Website:** <http://onsemi.com>

**Order Literature:** <http://www.onsemi.com/litorder>

For additional information, please contact your local Sales Representative.